defined by a plurality of coil conductor patterns arranged on the same plane of the insulating layers of the laminated body.

3. The delay line according to claim 8, wherein each of the at least three inductors has a coil axis that is substantially parallel with a laminating direction of the insulating layers of the laminated body, and winding directions of adjacent ones of the at least three inductors are opposite to each other.

4. The delay line according to claim 8, wherein the insulating layers are made of a dielectric ceramic material having a relative dielectric constant of about 15 or less.

5. The delay line according to claim 8, wherein one of the plurality of capacitors is connected to an end of at least one of the at least three inductors, and another of the plurality of capacitors is connected to another end of said at least one of the at least three inductors, are located at different positions in a laminating direction of the insulating layers.

6. A delay line comprising:

a coil divided into at least three inductors; and

a laminated body including a plurality of insulating layers and at least three stages of low pass filters including said at least three inductors and a plurality of capacitors; wherein

a ratio of a vertical dimension to a lateral dimension of each of the coil conductor patterns is approximately 1.

7. A delay line comprising:

a coil divided into at least three inductors; and

a laminated body including a plurality of insulating layers and at least three stages of low pass filters including said at least three inductors and a plurality of capacitors; wherein

one end of a first of the at least three inductors of a k stage in the low pass filter and one end of a second of the at least three inductors of a k+1 stage adjacent thereto in the low pass filter are electrically connected to each other on an upper layer of the laminated body, and the second end of the another of the at least three inductors of the k+1 stage in the low pass filter and one end of a third of the at least three inductors of a k+2 stage adjacent thereto in the low pass filter are electrically connected to each other on a lower layer of the laminated body.

8. A delay line comprising:

a coil divided into at least three inductors; and

a laminated body including a plurality of insulating layers and at least three stages of low pass filters including said at least three inductors and a plurality of capacitors; wherein

the coil is divided into at least four inductors.

9. The delay line according to claim 8, wherein the low pass filters are LC π type low pass filters.

10. The delay line according to claim 2, wherein the insulating layers have a plurality of via holes for connecting the coil conductor patterns that define the at least three inductors.

12. The delay line according to claim 8, wherein the number of the plurality of capacitors is greater than the number of the inductors.

13. A delay line comprising:

a coil divided into at least three inductors; and

a laminated body including a plurality of insulating layers and at least three stages of low pass filters including said at least three inductors and a plurality of

capacitors; wherein

the insulating layers include magnetic material.

15. The monolithic circuit array according to claim 20, wherein at least three inductors and at least four capacitors are included in the at least three stages of low pass filters.

16. The monolithic circuit array according to claim 20, wherein at least four stages of low pass filters are provided in the monolithic laminated body, and at least four inductors and at least five capacitors are included in the at least four stages of low pass filters.

17. The monolithic circuit array according to claim 20, wherein the inductors are defined by a plurality of coil conductor patterns arranged on the same plane of the insulating layers of the laminated body.

18. The monolithic circuit array according to claim 20, wherein the insulating layers are made of a dielectric ceramic material having a relative dielectric constant of about 15 or less.

19. The monolithic circuit array according to claim 20, wherein one of the capacitors is connected to an end of at least one of the inductors, and another of the capacitors is connected to another end of said at least one of the inductors, and the one of the capacitors and the another of the capacitors are located at different positions in a laminating direction of the insulating layers.

20. A monolithic circuit array including a delay line comprising:

a coil divided into at least three inductors; and

a plurality of insulating layers stacked on each other to define a monolithic laminated body, the laminated body including at least three stages of low pass filters

defined by lumped constant inductors and capacitors; wherein

a ratio of a vertical dimension to a lateral dimension of each of the coil conductor patterns is approximately 1.

21. The monolithic circuit array according to claim 20, wherein the low pass filters are LC π type low pass filters.

22. The monolithic circuit array according to claim 20, wherein the number of the plurality of capacitors is greater than the number of the inductors.